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| 10/511,855 | 03/29/2005 | Nicola Da Dalt | 10808/172 | 6363 |

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| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/511,855 | DA DALT, NICOLA | |
| | Examiner | Art Unit | |
| | Andrew O. Arena | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

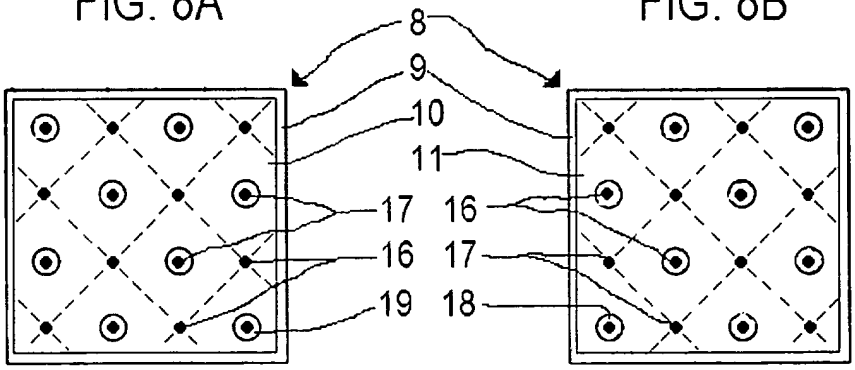
The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (US 6,370,010) in view of Arita (US 6,046,467).

Reference is made to the structure of Kuroda Fig 8, which is based on Figs 1-4 (col 8 ln 30-35, col 5 ln 58-59). Fig 8 is analogous to Fig 1, but there are no analogous drawings to Figs 3-4. Examiner has drawn and attached Figs 8A and 8B, which correspond to Figs 3A and 3B, for ease of reference in this rejection. In a similar manner, it is easy to picture the drawing corresponding to Fig 4, which is not shown.

FIG. 8A FIG. 8B



**Regarding claim 1**, Kuroda discloses a capacitance structure (Fig 8; col 8 ln 30-35) that comprises:

a first substructure (Fig 8A: 10; col 6 ln 9) which has a first cohesive latticed region including crossing metal leads (represented by dashed lines) which extends in a first common plane such that it has common top and bottom surfaces which limit the first cohesive latticed region in each of its subregions from above and from below,

wherein the first cohesive latticed metal region is electrically connected to a first connecting line (Fig 4&8A: 16); and

electrically conductive regions (Fig 8A: 17; col 6 ln 62-63) arranged in openings (Fig 8A: 19; col 7 ln 21) in the first cohesive latticed region of the first substructure at a distance from edge regions of the openings in the common plane,

wherein the electrically conductive regions are electrically connected to a second connecting line (Fig 4&8A: 17), and

wherein the electrically conductive regions comprise node points between via connections (Fig 8A: 17; col 7 ln 21).

**Further regarding claim 1**, Kuroda differs from the claimed invention in not expressly disclosing the cohesive latticed region is metal. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the cohesive latticed region from metal; at least because it is a common electrode material.

**Further regarding claim 1**, Kuroda differs from the claimed invention only in not expressly disclosing the capacitor is formed in a semiconductor component. Arita discloses (Fig 1) a semiconductor component (col 2 ln 53) comprising a semiconductor

substrate (21; col 2 ln 59) having an insulating layer (21a+26; col 2 ln 58-59, col 3 ln 31-34) on the semiconductor substrate surface and having a capacitance structure (25; col 3 ln 2-4) in the insulating layer, wherein the capacitance substructures (22-24) are parallel to the substrate surface. It would have been obvious to a person of ordinary skill in the art at the time of the invention provide the capacitance structure of Kuroda as the capacitor in the device of Arita; at least for the purpose of very low equivalent series inductance (ESL: Kuroda col 3 ln 19-21).

**Regarding claim 2**, Kuroda discloses the capacitance structure further comprises:

a second substructure (Fig 8B: 11; col 6 ln 9-10) parallel to and at a distance from the first substructure (col 6 ln 6-10; Fig 4, 8A) wherein the second substructure comprises:

a second cohesive latticed metal region including crossing metal leads (dashed lines in Fig 8B) which extends in a second common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region in each of its subregions from above and below; and

electrically conductive regions (Fig 8B: 16),

wherein the first and second substructures are electrically connected by the first (Fig 4&8A: 16) and second (Fig 4&8A: 17) connecting lines.

**Regarding claim 3**, Kuroda discloses the second substructure is of substantially the same design as the first substructure (col 6 ln 12-19), and the first and second substructures are laterally offset from one another (col 6 ln 15; lattices are clearly offset

in Figs 3A&3B and 8A&8B) such that the electrically conductive regions (Fig 8A: 17) of the first substructure are arranged vertically above (Fig 4) crossing points (Fig 8B: 17) of the metal leads in the second cohesive latticed metal region of the second substructure, and crossing points (Fig 8A: 16) in the first cohesive latticed metal region of the first substructure are arranged vertically above (Fig 4) electrically conductive regions (Fig 8B: 16) of the second substructure.

**Regarding claim 4**, Kuroda discloses wherein the crossing points (Fig 8A: 16) of the metal leads in the first cohesive latticed metal region of the first substructure are electrically connected to the electrically conductive regions (Fig 8B: 16) of the second substructure (col 6 ln 60-63), and the electrically conductive regions (Fig 8A: 17) of the first substructure are electrically connected to the crossing points (Fig 8B: 17) of the metal leads in the second cohesive latticed metal region of the second substructure (col 6 ln 64-67) by means of at least one respective via connection (16&17; col 6 ln 60, 63).

**Regarding claim 5**, Kuroda discloses wherein the second cohesive latticed metal region of the second substructure is laterally offset (col 6 ln 15; lattices are clearly offset in Figs 3A&3B and 8A&8B) from the first substructure so that the electrically conductive regions (Fig 8A: 17) of the first substructure are arranged vertically above (Fig 4) crossing points of the metal leads in the second cohesive latticed metal region (Fig 8B: 17) of the second substructure.

**Regarding claim 6**, Kuroda discloses wherein the electrically conductive regions (Fig 8A: 17) of the first substructure and the crossing points (Fig 8B: 17) of the metal leads in the second cohesive latticed metal region of the second substructure are

electrically connected (col 6 ln 64-67), by means of at least one respective via connection (16&17; col 6 ln 60, 63).

**Regarding claim 7**, Kuroda discloses a metal plate (bottom most 10 in Fig 4) electrically connected (col 6 ln 60-63) to one of the crossing points (Fig 8A: 16) of the metal leads in the cohesive latticed region of the first substructure (10) and to the electrically conductive regions (Fig 8B: 16) of the second substructure (11) by means of one or more respective via connections (16; col 6 ln 60-63).

**Regarding claim 8**, Kuroda discloses wherein the first cohesive latticed metal region has at least two round openings (Figs 3A&3B and 8A&8B).

**Regarding claim 9**, Kuroda discloses the first and second connecting lines are at different electric potentials (inherent in a capacitor; also col 6 ln 60-67) .

**Regarding claim 10**, Kuroda discloses a first non-parasitic capacitance exists between the cohesive latticed metal region of the first substructure and a second non-parasitic capacitance exists between the first and second connecting lines, and wherein the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance (inherent in disclosing applicant's claimed structure).

**Regarding claim 11**, Kuroda discloses a capacitance structure (Fig 8; col 8 ln 30-35) that comprises:

a first lattice (Fig 8A: 10) including intersecting leads (represented by dashed lines) in a first common plane;

a second lattice (Fig 8B: 11) including intersecting leads (represented by dashed lines) in a second common plane;

electrically conductive regions (Fig 8A: 17; Fig 8B: 16) arranged in openings in the first and second lattices [respectively], the electrically conductive regions spaced apart from edge regions of the opening by [an] insulation layer (Fig 4: 9; col 6 ln 11, 61, 64); and

wherein the first and second lattices are laterally offset from one another (col 6 ln 15; lattices are clearly offset in Figs 3A&3B and 8A&8B), such that the electrically conductive regions of the first lattice (Fig 8A: 17) are substantially vertically above crossing points of the second lattice (Fig 8B: 17), and crossing points of the first lattice (Fig 8A: 16) are substantially vertically above the electrically conductive regions of the second lattice (Fig 8B: 16); and

first (17) and second (16) electrical connections between the first and second lattices (Fig 4, col 6 ln 60-67) such that the first and second electrical connections are at different electrical potential (inherent in a capacitor).

**Further regarding claim 11**, Kuroda differs from the claimed invention in not expressly disclosing the lattices are metal. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the lattices from metal; at least because it is a common electrode material.

**Further regarding claim 11**, Kuroda differs from the claimed invention only in not expressly disclosing the capacitor is formed in a semiconductor component. Arita discloses (Fig 1) a semiconductor component (col 2 ln 53) having an integrated capacitance structure, the component comprising:

a semiconductor substrate (21; col 2 ln 59) having a surface;

an insulating layer (21a+26; col 2 ln 58-59, col 3 ln 31-34) overlying the surface of the semiconductor substrate;

a capacitance structure (25; col 3 ln 2-4) in the insulating layer, wherein the capacitance substructures (22-24) are parallel to the substrate surface. It would have been obvious to a person of ordinary skill in the art at the time of the invention provide the capacitance structure of Kuroda as the capacitor in the device of Arita; at least for the purpose of very low equivalent series inductance (ESL: Kuroda col 3 ln 19-21).

**Regarding claim 12**, Kuroda discloses the electrically conductive regions comprise node points (Fig 8A: 17; col 7 ln 21).

**Regarding claim 13**, Kuroda discloses the electrical connections comprise:

first connecting lines (17) electrically connecting the electrically conductive regions of the first metal lattice (Fig 8A: 17) to crossing points of the second metal lattice (Fig 8B: 17); and

second connecting lines (16) electrically connecting crossing points of the first metal lattice (Fig 8A: 16) to the electrically conductive regions of the second metal lattice (Fig 8B: 16).

**Regarding claim 14**, Kuroda discloses a metal plate (bottom most 10 in Fig 4) in a third common plane parallel to the substrate surface and electrically coupled to the first and second metal lattices by the first and second electrical connections (all features in a common capacitor are electrically coupled).

**Regarding claim 15**, Kuroda discloses a third metal lattice (bottom most 10 in Fig 4) including intersecting metal leads (represented by dashed lines in Fig 8A&8B) in

a third common plane parallel to the substrate surface, wherein the intersecting metal leads define openings (donut shaped opening 19 lying between 10 and 17), wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections (16 and 17; col 6 ln 60-67).

**Regarding claim 16**, Kuroda discloses a capacitance structure (Fig 4 & 8; col 8 ln 30-35) that comprises:

an insulating layer (Fig 4: 9; col 6 ln 11);

a first lattice (Fig 8A: 10) in the insulating layer, the first lattice including intersecting leads (represented by dashed lines) in a first common plane;

a second lattice (Fig 8B: 11) in the insulating layer , the second lattice including intersecting leads (represented by dashed lines) in a second common plane;

electrically conductive regions (Fig 8A: 17; Fig 8B: 16) arranged in openings in at least one of the first and second lattices, the electrically conductive regions spaced apart from edge regions of the opening by the insulation layer (Fig 4: 9; col 6 ln 61); and

wherein the first and second lattices are laterally offset from one another (col 6 ln 15; lattices are clearly offset in Figs 3A&3B and 8A&8B), such that the electrically conductive regions of the first lattice (Fig 8A: 17) are substantially vertically above crossing points of the second lattice (Fig 8B: 17), and crossing points of the first lattice (Fig 8A: 16) are substantially vertically above the electrically conductive regions of the second lattice (Fig 8B: 16);

a third structure (bottommost 10 in Fig 4) in the insulating layer in a third common plane, the third metal structure comprising a third lattice; and

first (17) and second (16) electrical connections between the first and second lattices (Fig 4, col 6 ln 60-67) such that the first and second electrical connections are at different electrical potential (inherent in a capacitor).

**Further regarding claim 16**, Kuroda differs from the claimed invention in not expressly disclosing the lattices are metal. However, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form the lattices from metal; at least because it is a common electrode material.

**Further regarding claim 16**, Kuroda differs from the claimed invention only in not expressly disclosing the capacitor is formed in a semiconductor component. Arita discloses (Fig 1) a semiconductor component (col 2 ln 53) having an integrated capacitance structure. It would have been obvious to a person of ordinary skill in the art at the time of the invention provide the capacitance structure of Kuroda as the capacitor in the device of Arita; at least for the purpose of very low equivalent series inductance (ESL: Kuroda col 3 ln 19-21).

**Regarding claim 17**, Kuroda discloses the third metal structure comprises a metal plate electrically coupled to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections (all features in a common capacitor are electrically coupled).

**Regarding claim 18**, Kuroda discloses the third metal structure comprises a third metal lattice (bottommost 10 in Fig 4) including intersecting metal leads

(represented by dashed lines in Fig 8A&8B), wherein the intersecting metal leads define openings (donut shaped opening 19 lying between 10 and 17), wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections (16 and 17; col 6 ln 60-67).

**Regarding claim 19**, Kuroda discloses wherein the first electrical connection (17) electrically connect the electrically conductive regions of the first metal lattice (Fig 8A: 17) to the crossing points of the second metal lattice (Fig 8B: 17), and wherein the second electrical connection (16) electrically connect the crossing points of the first metal lattice (Fig 8A:16) to the electrically conductive regions of the second metal lattice (Fig 8B: 16).

**Regarding claim 20**, Kuroda discloses the third metal structure comprises a third metal lattice (bottommost 10 in Fig 4) including intersecting metal leads (represented by dashed lines in Fig 8A&8B) and electrically conductive regions (Fig 8A: 17) in openings defined by the intersecting metal leads.

**Regarding claim 21**, Kuroda discloses non-parasitic capacitances exist between the electrically conductive regions and intersecting metal leads in the first, second, and third metal lattices and wherein non-parasitic capacitances exist between the first and second connecting lines (inherent in disclosing applicant's claimed structure).

***Response to Arguments***

Applicant's arguments filed 02/02/2006 have been fully considered but they are not persuasive.

Applicant's argument that "Kuroda does not suggest or disclose a capacitor structure that includes crossing metal leads" is not persuasive. Applicant's figure 4 and Kuroda figure 3 both depict a plurality of overlying metal sheets including openings, wherein linear portions uninterrupted by openings are regarded as leads. Applicant's figure 4 and Kuroda figure 3 are thus structurally identical; in the same way that applicant depicts 'crossing metal leads', Kuroda depicts the same.

Applicant's argument that "Kuroda does not suggest or disclose different regions of a first substructure in which separate connecting lines are electrically connected to the different regions" is not persuasive. Kuroda discloses (Fig 4, 8A & 8B) a substructure (Fig 8A: 8) comprising both conductive regions (Fig 8A: 17) and a latticed region (Fig 8A: 10) in which separate connecting lines (17, 16; col 6 ln 60-67) are electrically connected to the different regions.

Applicant's argument that "there is no suggestion within Kuroda for a lattice structure or for the cross-hatched representation" is moot, since Kuroda discloses applicant's claimed capacitance structure, and the cross-hatched lines are not relied upon, but merely illustrate existing portions of the structure disclosed by Kuroda.

Applicant's argument that "such an alignment relationship is not suggested or disclosed by Kuroda" is not persuasive since Kuroda discloses applicant's claimed capacitance structure.

## *Conclusion*

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOA
21 April 2006

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